OTC24000 Datasheet Rev 1.0

Dynamically Reconfigurable Analog Matrix With Enhanced I/O

www.okikatechnologies.com

Disclaimer

Okika Technologies reserves the right to make any changes without further notice to any products herein. Okika Technologies makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Okika Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Okika Technologies does not in this document convey any license under its patent rights nor the rights of others. Okika Technologies software and associated products cannot be used except strictly in accordance with an Okika Technologies software license. The terms of the appropriate Okika Technologies software license shall prevail over the above terms to the extent of any inconsistency.

PRODUCT AND ARCHITECTURE OVERVIEW

The OTC24000 device is an “Analog Signal Processor”; ideally suited to signal conditioning, filtering, gain, rectification, summing, subtracting, multiplying, etc. The device also accommodates nonlinear functions such as sensor response linearization and arbitrary waveform synthesis.

The OTC24000 device consists of a 2x2 matrix of fully Configurable Analog Blocks (CABs), surrounded by programmable interconnect resources and analog input/output cells with active elements. On chip clock generator block controls multiple non-overlapping clock domains generated from an external stable clock source. An internal band-gap reference generator is used to create temperature compensated reference voltage levels. The inclusion of a 256x8 bit look-up table enables waveform synthesis and several non-linear functions.

Configuration data is stored in an on-chip SRAM configuration memory. An SPI-like interface is provided for simple serial load of configuration data under firmware control from a microprocessor or DSP, or automatically by the OTC24000 at power up from a SPI EEPROM. The SRAM configuration memory is shadowed allowing a different circuit configuration to be loaded as a background task without disrupting the current circuit functionality.

The OTC24000 device features seven configurable I/O structures: each can be used as input or output, 4 of the 7 have integrated differential amplifiers. There is also a single chopper stabilized amplifier that can be used by 3 of the 7 output cells.

Circuit design and configuration is enabled using Dynamx Design Lab software, a high level block diagram based circuit design entry and simulation tool. Circuit functions are represented as CAMs (Configurable Analog Modules) these are configurable block which map onto portions of CABs. The software and a development board facilitate instant prototyping of any circuit captured in the tool.

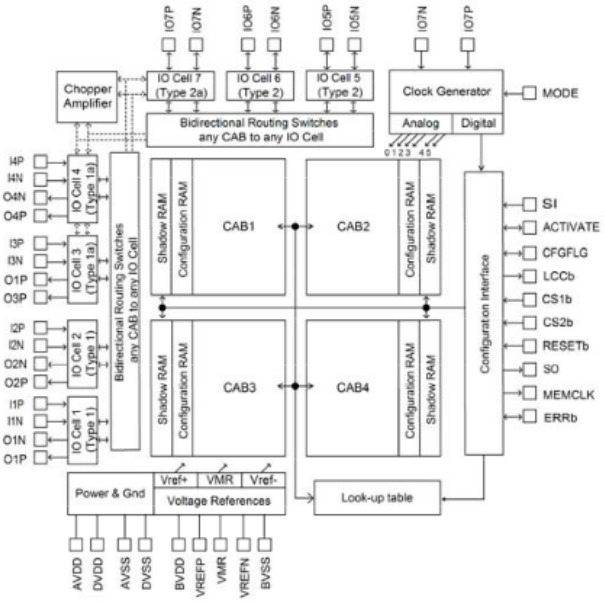


Figure 1: Architectural overview of the OTC24000 device

With dynamic reconfigurability, the functionality of the OTC24000 can be reconfigured in-system by the designer or on-the-fly by a microprocessor. A single OTC24000 can thus be programmed to implement multiple analog functions and/or to adapt on-the-fly to maintain precision operation despite system degradation and aging.

PRODUCT FEATURES

- **Dynamic reconfiguration**
- Four configurable I/O cells, two dedicated output cells
- 8-bit SAR analog–to–digital converter
- Fully differential architecture
- Fully differential I/O buffering with options for single ended to differential conversion
- Low input offset through chopper stabilized amplifiers
- 256 Byte Look-Up Table (LUT) for linearization and arbitrary signal generation
- 4:1 Input multiplexer
- Typical Signal Bandwidth: DC-2MHz (Bandwidth is CAM dependent)
- Signal to Noise Ratio:
  - Broadband 80dB
  - Narrowband (audio) 100dB
- Total Harmonic Distortion (THD): 80dB
- DC offset <100µV
- Package: 44-pin QFP (10x10x2mm)
  - Lead pitch 0.8mm
- Supply voltage: 3.3V

APPLICATIONS

Intelligent sensors
Ultrasound
Adaptive filtering and control
Adaptive DSP front-end
Adaptive industrial control and automation
Self-calibrating systems
Compensation for aging of system components
Dynamic recalibration of remote systems
Ultra-low frequency signal conditioning
Custom analog signal processing

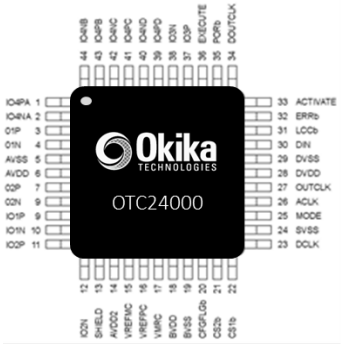


Table of Contents

Architecture Overview

Important Note:

The Okika Technologies OTC24000 device is a complex configurable analog circuit that is intended to be used in conjunction with our Dynamx Design Lab design and simulation software. That software fully automates the process of designing and configuring the OTC24000 as well as generating configuration data files and C code for user host controller applications. Okika does not recommend users attempting to generate data files outside of the Dynamx Design Lab environment without support. The Dynamx Design Lab environment includes an extensive library of Configurable Analog Modules that may be used in the schematic editor and simulator to build complex circuits. The user can then focus on system requirements, design, quick-prototyping, and design verification and then leave the complexities of configuration data generation and management to the Okika software tools. For more information visit the Okika Technologies download site to access the latest version of design support software.

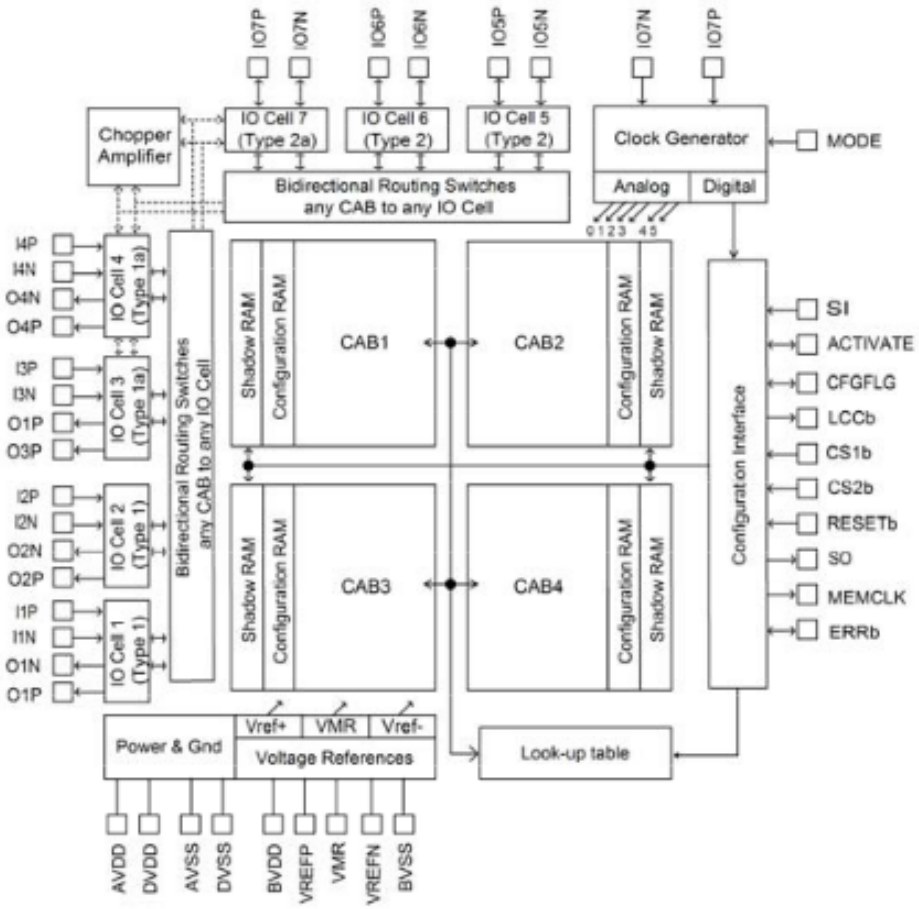


Figure 1 – Overview of the OTC24000 dynamically programmable Analog Signal Processor Architecture

The Okika Technologies OTC24000 processes analog signals in their IO Cells and Configurable Analog Blocks (CABs). These structures are constructed from a combination of conventional and switched capacitor circuit elements and are programmed from off-chip non-volatile memory or by a host processor. This Field Programmable Analog Array (FPAA) enables adaptability and flexibility in analog circuits not previously possible.

The SRAM based OTC24000 device is *dynamically reconfigurable*. The behaviour of the FPAA can be modified partially or completely while operating. Dynamic Reconfiguration allows a companion host processor to send

new configuration data to the FPAA while the old configuration is running. Once the new data load completes, the transfer to the new analog signal processing configuration happens in a single clock cycle. Dynamic Reconfiguration in the OTC24000 device allows the user to develop innovative analog systems that can be updated (fully or partially) on-the-fly, as often as needed.

OTC24000 FPAAs contain 4 Configurable Analog Blocks (CABs) in their cores. Most of the analog signal processing occurs within these CABs and is done with fully differential switched capacitor circuitry. The CABs share access to a single Look Up Table (LUT) that offers a method of adjusting any programmable element within the device in response to a signal or time base. The LUT can also be used to implement arbitrary input-to-output transfer functions (companding, sensor linearization), generate arbitrary signals, and construct voltage dependent filtering. A Voltage Reference Generator supplies reference voltages to each of the CABs within the device and has external pins for the connection of filtering capacitors.

Analog signals are routed in and out of the FPAA core via the available IO cells: two Type 1, two Type 1a, two Type 2, and one Type 2a. Type 1 and Type 1a IO cells contain both passive and active circuitry which allows direct signal input and output, building of active filters, sample and hold circuits, digital inputs, and digital outputs. The response of continuous time input and output filters is determined by a combination of internal programming and external components.

Type 2 and Type 2a IO cells are simpler and can implement direct input and output, reference voltage output, digital input, and digital output.

Any one of the Type 1a or Type 2a IO cells can have access to a specialized chopper amplifier resource which allows accurate amplification of very low energy inputs signals.

Look-Up Table (LUT) functionality facilitates the construction of arbitrary waveform generators and non-linear transfer functions. On-chip voltage reference generation precludes the need of any external reference voltage generation circuitry.

The design of circuits for the FPAA is accomplished using Okika Technologies' Dynamx Design Lab software. This software presents a graphical circuit design environment in which basic analog signal processing building blocks are dropped into place and wired together. Building blocks include: gain, filter, summing, rectification and many other more specialized behaviours. Specific parameters for each of the blocks used (e.g. Gain, Corner Frequency, etc.) are set by the user. Okika Technologies Dynamx Design Lab generates a configuration data file. The FPAA's configuration data file can be used to program a SPI PROM for stand-alone static operation, or compiled into a microcontroller's source program for hosted dynamic operation.

Okika Technologies Dynamx Design Lab also generates C source code for a host microcontroller which enables on-the-fly generation of new FPAA configuration data and subsequent dynamic reconfiguration. The FPAAs' signal processing behaviour can be adjusted while your system remains continuously in mission mode.

The behaviour of the analog circuitry is controlled by the contents of the FPAA's configuration memory. This memory is SRAM-based and must be programmed after power-up. The FPAA's configuration interface provides a data port for this purpose. The configuration interface presents itself as a slave serial data port to a companion microprocessor, compatible with SPI signalling. The configuration interface can otherwise be configured to read data from an attached SPI PROM automatically after power-up or a device reset.

Typical Configuration Interface Connections

The behaviour of the analog signal processing circuits within an OTC24000 device is dictated by the contents of its volatile (SRAM based) configuration memory. At power-on-reset, the FPAA clears its memory, placing the device in a benign condition. Once this power-on-reset sequence concludes, the device is ready to accept configuration data. The first configuration data set loaded into the device after a reset is called a Primary Configuration.

OTC24000 devices may be Reconfigured (without intervening resets) using the Update format described later.

The configuration interface presents itself as either a serial data master or serial data slave. As a serial data master, the FPAA can automatically retrieve its configuration data set from any industry standard SPI PROM attached. As a serial data slave, the FPAA is compatible with SPI signalling from a host processor and can accept its configuration data from that host.

Dynamic Operation

The most powerful application scheme is when the FPAA is configured as a serial data slave. In this Dynamic Operation a companion host processor sends configuration data to the FPAA using SPI compatible signaling. This allows the creation of analog signal processing circuits that can be changed on-the-fly. The change may be as simple as a minor adjustment of a gain or corner frequency, or may involve wholesale transformation of behavior, say from a transmitter to a receiver configuration.

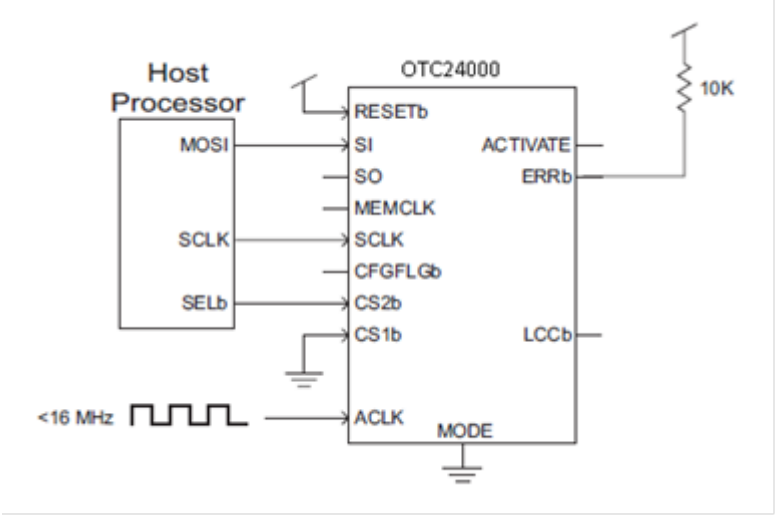


Figure 2 – Configuring a single FPAA from a Host Processor

Out of power-on-reset, the FPAA remains in a benign state, waiting for a configuration sequence. In order to configure the FPAA, the host processor drives CS2b low then streams a configuration data set out of its serial data port. Normally, the FPAA will enable analog signal processing automatically at the conclusion of configuration, though other options are discussed below.

Static Operation

In static operation, the FPAA will automatically read in its configuration data from an SPI EEPROM after a manual reset or on power-up.

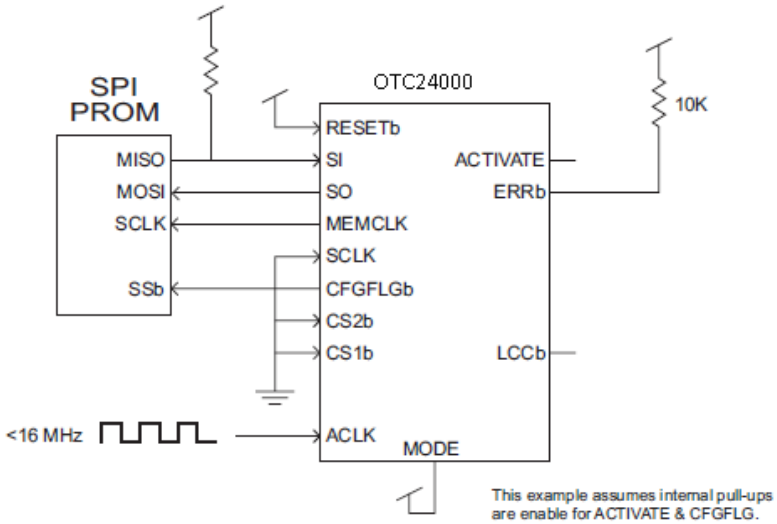


Figure 4 – A single FPAA self-configuring from a SPI EEPROM

At the conclusion of the power-on-reset sequence, CFGFLGb will be low, selecting the attached SPI PROM. The standard "read" command will be issued out of SO (clocked by MEMCLK). As MEMCLK continues, the SPI PROM responds with a serial data stream. This serial data stream is read by the SI pin.

Normally, the FPAA will enable analog signal processing automatically at the conclusion of configuration, though other options are discussed in more detail below.

In this simplest use model, the FPAA automatically: detects power-on, resets itself, reads in configuration data from a standard SPI PROM, and begins analog signal processing. A subsequent reset or power cycle will cause the sequence to repeat.

A slightly more advanced application of static configuration allows for the connection of several FPAA's to a single SPI PROM. In this use scenario, the FPAAs are daisy chained; the *upstream* (closer to the PROM) device's Local Configuration Complete (LCCb) pin feeds the *downstream* device's CS1b enable pin. The SPI PROM's MISO data output pin is bussed to all FPAAs. All FPAA's have their ACTIVATE and ERRb pins commoned.

As with the single FPAA example, the first FPAA in the chain still provides the "read" command to the SPI PROM but provides the necessary clocking for *all* the serial configuration data. As the configuration completes for an *upstream* device, its LCCb asserts low and enables the next device in the chain (*downstream)* to receive its data.

ACTIVATE is an open-drain bidirectional pin. During configuration the ACTIVATE pin is asserted low. Analog circuitry is not enabled (activated) until the ACTIVATE pin moves to a high state. As the local configuration completes, the FPAA de-asserts its ACTIVATE pin and monitors the ACTIVATE node. The daisy chained LCCb to CS1b sequence continues until all FPAAs in the chain have received configuration data. At that point all of the FPAAs will have de-asserted ACTIVATE and the commoned line will pull-high. Tying the ACTIVATE pin of all the devices in the configuration chain together ensures that analog signal processing does not begin in any of the FPAAs until all of them have received their configuration data.

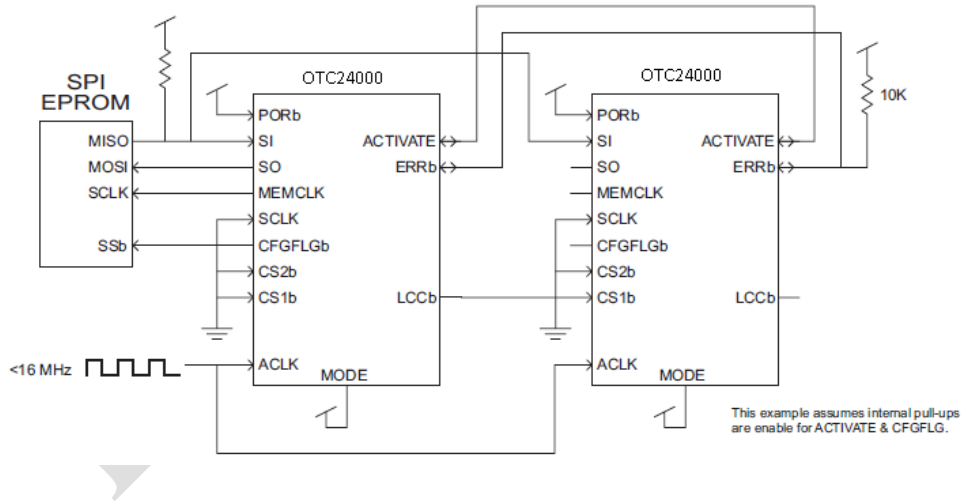


Figure 5 – Multiple FPAAs self-configuring from a single SPI PROM

ERRb is also an open-drain bidirectional pin. The ERRb pin will assert low if illegal or corrupted data is detected. Tying the ERRb pin of all the devices in the configuration chain together ensures that if any device detects an error, then all of the devices in the chain will reset (including the SPI PROM) and the configuration sequence will re-start automatically.

The following are important notes regarding the SPI and configuration signal connections:

Pull-Ups on SI
Most SPI EPROMs hold their MISO pin in tri-state when the device is not selected. In order to ensure a valid logic signal is always presented to the FPAA a pull-up on the SI node is recommended.

Pull-Ups on ERRb
A 10k resistor is always required on the ERRb node.

Pull-Ups on ACTIVATE
The ACTIVATE pin has a programmable internal pull-up. In Master mode systems in which there are 3 or fewer FPAAs, it is recommended that the most upstream device enable its ACTIVATE pull-up. Master mode systems constructed with 4 or more FPAAs should use only an external pull-up on the ACTIVATE node.

Pull-Ups on CFGFLGb
The CFGFLGb pin has a programmable internal pull-up. The internal pull-ups for CFGFLGb and ACTIVATE are controlled with a single configuration bit; they are not separately programmable. Conse- quently, the same pull-up rules for ACTIVATE apply here to CFGF

Configuration Interface Details

Pin Descriptions

MODE

The state of the MODE pin is read as part of the FPAA's power-on-reset sequence. If MODE is low out of reset the configuration interface establishes itself as a serial data slave. If MODE is high, the config- uration interface establishes itself as a serial data master. MODE should either be tied high to VDD or low to VSS. This is a static pin. Changing its state after power up is not allowed.

For more details on the effects of MODE, see section 4.2.4.

SCLK (Serial Clock)

If MODE is low, SCLK serves as the serial data clock input. The configuration state machine is driven from this input. SCLK may not exceed 40 MHz. SCLK may be free running or discontinuous.

If MODE is high, then SCLK is ignored and the configuration state machine is driven from an internally divided down ACLK (ACLK/16).

MEMCLK (Memory Clock)

If MODE is high, the FPAA establishes itself as a serial data master. MEMCLK serves as the serial data clock output.

Once configuration is complete, the MEMCLK pin may be used as a user programmable digital output.

ACLK (Analog Clock)

ACLK is the input for the analog clock source. All internal switched capacitor clocks are derived from the ACLK input. ACLK may not exceed 40 MHz.

If MODE is high, then SCLK is ignored and the configuration state machine is driven from an internally divided down ACLK (ACLK/16).

SI (Serial In)

The SI pin always serves as the configuration data input pin.

SO (Serial Out)

When MODE is high, the SO pin issues the “read” command to the attached SPI PROM.

LCCb (Local Configuration Complete)

LCCb (Local Configuration Complete) is high during power-on-reset and remains high until the local configuration completes, it then goes low.

In multi-FPAA systems, LCCb is normally connected to the CS1b input of the next FPAA down- stream.

Once configuration is complete, the LCCb pin may be used as a user programmable digital output. LCCB is active low.

CS1b (Chip Select 1)

The CS1b pin also serves as a chip select input, but its behavior is more involved than CS2b. In mul- tiple FPAA systems, the CS1b input is normally driven by the upstream device’s LCCb pin. Out of reset, the LCCb pin of the upstream device will be high - suspending the configuration of the down- stream device. Once the upstream device completes its local configuration and drives its LCCb low, the downstream device will begin its configuration. CS1b is active low.

CS2b (Chip Select 2)

The CS2b pin serves as a regular chip select input. CS2b is active low.

CFGFLGb (Configuration Flag)

When connecting multiple FPAAs up as suggested in Figure 15, it is necessary to tie the CFGFLGb pins of the devices to a common node. The CFGFLGb node will be driven low whenever a device is being addressed for configuration or reconfiguration (AN23x devices only) and will pull-high when data transfer is complete. When the local device senses CFGFLGb as being pulled low (by another device), the local device ignores the data on SI. This CFGFLGb signaling prevents reconfiguration data intended for one device from being wrong intercepted by another.

There is a single configuration data bit which enables of the CFGFLGb and ACTIVATE internal pull-up resistors.

ERRb (Error)

ERRb is an open-drain, bidirectional pin. The pin asserts low whenever a configuration error is detected.

In multi-FPAA systems, the ERRb pins should all be commoned. When the local device senses ERRb as being pulled low (by another device), the local device resets. Also, the ERRb signal is an enabling

term in the power-on-reset cycle. Commoning the ERRb pins in a multi-FPAA system allows all the devices to complete their POR sequences concurrently (though not all device types complete their power-on-reset cycles in the same amount of time). More complete details on the behaviors associated with this pin are deferred to section 4.2.2.

ERRb must be pulled high with an external pull-up resistor. 10 K_W is the usual value, but may be less if the node is heavily loaded. ERRb is active low.

ACTIVATE

ACTIVATE is an open-drain, bidirectional pin. In a single FPAA system, ACTIVATE can be left floating. During a primary configuration, the ACTIVATE pin is asserted low. When the primary configuration is complete, ACTIVATE is release and monitored. When ACTIVATE is sensed as high, analog processing circuits are *activated*.

In multi-FPAA systems, the ACTIVATE pins are all commoned. When the local device completes its configuration, it quits driving ACTIVATE low and then monitors the state ACTIVATE line. Once all devices have completed their configuration, the ACTIVATE node will finally go high, allowing all devices to activate analog signal processing concurrently. More complete details on the behaviors associated with the ACTIVATE function are deferred to section 4.3.2.

There is a single configuration data bit which enables of the CFGFLGb and ACTIVATE internal pull-up resistors.

RESETb

RESETb is an active low input. Normally the RESETb is tied high; internal power-on-reset circuitry senses brown-out or power up conditions and automatically resets the device. If the application dictates a manual reset capability, the pin may be driven low then high to re-initiate a complete power-on reset sequence.

Special Functions - Configuration and Control Features

Resets

There are two classes of reset in the device. A Primary Reset brings the configuration logic into a safe starting condition and clears all Shadow and Configuration SRAM with the exception of the LUT. A Secondary Reset only brings the configuration logic into a reset condition; all SRAM contents are left undisturbed.

During power-up, power-on-reset circuitry initiates a Primary Reset. This same circuitry initiates a Primary Reset whenever brown out conditions occur or the external RESETb pin is driven low. Holding the RESETb pin low keeps the device in reset until released.

A Secondary Reset only resets the configuration logic; no SRAM contents are affected. The sources of Secondary Resets are: Software Reset (see section 5.1.3 for further details) and a long ERRb pulse (see section 4.2.2 for further details).

ERRb

The ERRb pin serves several different functions.

As an output, a low asserted ERRb indicates a configuration error. If a configuration data error is detected during a Primary Configuration, ERRb will assert low for 19 configuration clock cycles. (19 SCLK cycles in Slave mode or 240 ACLK cycles in Master mode. Recall that ACLK/16 drives the configuration logic in Master mode.) The ERRb response to a configuration data error during a reconfiguration (AN23x devices only) is programmable. On error detection, the low assertion of ERRb may be for either 5 or 19 configuration data clocks. A “short” ERRb pulse indicates that the local device detected an error and that a reset occurred. A “long” ERRb pulse will cause all devices tied to the common ERRb node to reset.

As an input, holding ERRb low for 19 (or more) configuration clock cycles will cause a Secondary Reset. (Pulsing RESETb low is the recommended method for manually asserting a reset.)

ERRb is also a controlling term which holds off the completion of a power-on-reset sequence. Early in the power-on-reset sequence, ERRb is asserted low. Late in the power-on-reset sequence, ERRb is released and monitored. When ERRb reaches a valid logic high state, the power-on-reset sequence concludes. Since not all FPAA device types have the same length power-on-reset sequence, commoning the ERRb pins of all of the FPAAs within a system ensures that all devices will remain in reset until the slowest device finishes, at which point all the devices will come out of reset concurrently. (See section 4.2.1 for furtherdetails.)

Watchdog

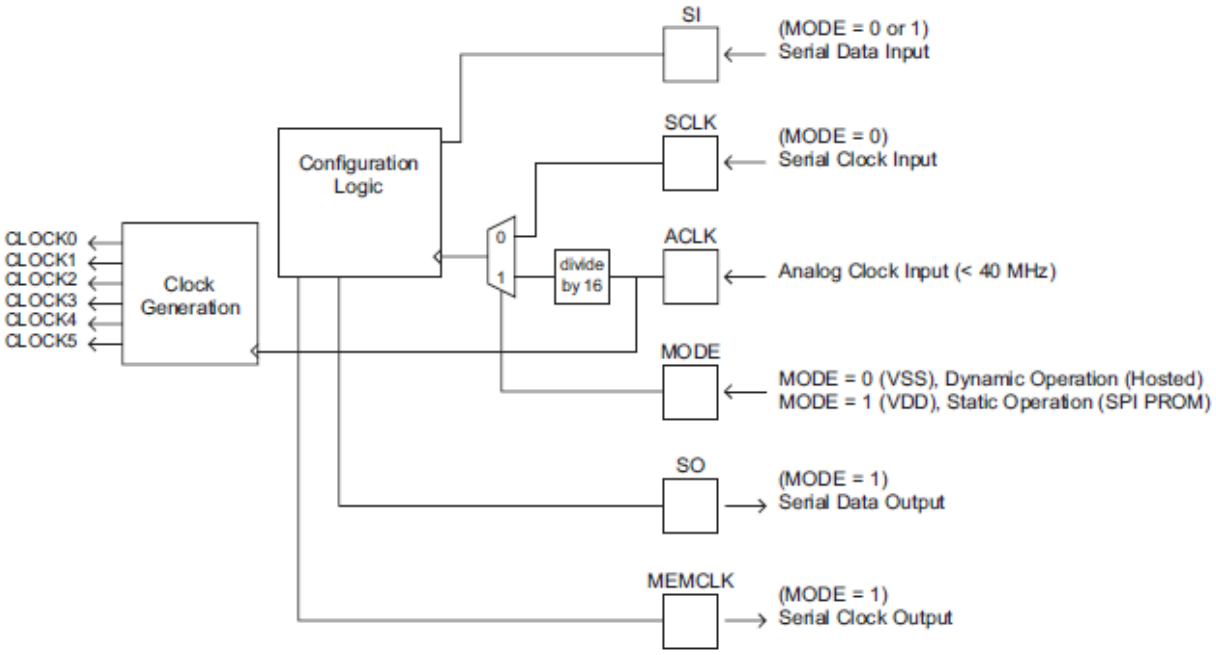
The device contains an automatic power savings feature. When enabled, this Watchdog circuit monitors the frequency of the primary analog clock (ACLK pin). When ACLK falls below 31.25 KHz, the device will auto- matically shift into a powered-down condition. Resumption of ACLK will immediately bring the part back up into a normal powered state, though how fast normal signal processing resumes is a function of the current CAB configurations.

Analog and Configuration Clock Generation

All signal processing clocks within the device are derived from the analog master clock signal presented on the ACLK pin. The ACLK signal gets split and divided down into two system base clocks (SYS1 and SYS2), the divisor being between 1 and 510. These two system clocks are further divided down into 6 additional clock domains: Clock 0 through Clock 5. Each of these 6 analog processing clocks can use either SYS1 or SYS2 as its base, and will further divide that base clock down by 1 up to 510. Clock 5 and Clock 6 have an arbitrary phase delay setting which ranges from 0° to 360°.

Having two base clocks allows for creation of two unrelated analog signal processing circuits within a single device.

Clock frequency is a fundamental parameter in the function of switched capacitor analog circuitry. If clock frequencies are changed later in the course of the design, care must be taken to ensure that the CAMs with frequency parameters placed in the design are still operating as desired. For example, changing the frequency of the clock driving a filter CAM will change the frequency response of that filter.



Analog Architecture Details

Important note: like all configurable functions on the OTC24000, input/output cells are configured using the DynAMx Design Lab software tools available at Okika Technologies' website.

Types 1 and 1a IO Cells

The device contains two Type 1 and two Type 1a IO cells. These IO sites provide tremendous flexibility in getting signals in and out of the CABs. Available options are summarized below:

Bypass I/O
- Differential Input
- Differential Output

Digital I/O
- Differential Input
- Differential Output

Analog Input
- Amplifier, or
- Differential Low Offset Chopper Amplifier (type 1a IO cell only), or
- Sample and Hold, with options forinput:
  - Differential
  - Inverted Differential
  - Single Ended Positive
  - Single Ended Negative

Analog Output
- Differential Amplifier
- Differential Sample and Hold

VMR Output
- Internal signal reference (1.5 V) presented on both pins.

Bypass

The Bypass setting of the IO cells provides direct, unbuffered access to CAB input and output ports. When using Bypass inputs, care should be taken to ensure that the differential signal and reference voltages are compatible with the CAB. Differential voltages should be maintained between 0 and 3 V, and centered about VMR (1.5 V).

Digital

Differential logic buffers are available to get signals into and out of the array. This IO configuration is most often used with Comparator and ADC-SAR CAMs.

Analog Input

The Amplifier's outputs are presented to the external pins for construction of anti-aliasing filters and external gain control.

The Sample and Hold setting provides a sampling circuit which can be used with either phase of the IO cell's clock. The Sample and Hold input can be configured as: Differential, Inverted Differential, Single Ended Positive, or Single Ended Negative.

On Type 1a IO cells, a Low Offset Chopper Amplifier setting is available. The Chopper Amplifier is spe- cially designed to provide very low offset voltages for weak external signals which must be gained up prior to processing in the CAMs. This setting includes programmable gain from 0, to 40 dB in 10 dB steps.

Analog Output

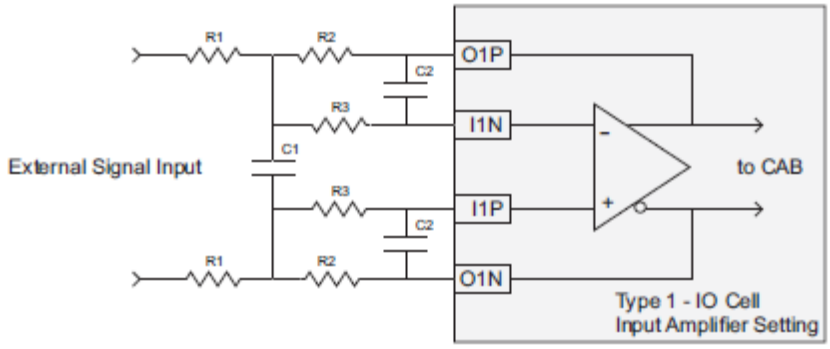
Similar to Analog Input, Analog Output settings include: Amplifier, and Sample and Hold. Signalling from an Analog Output is always differential. The Amplifier setting of Analog Output is unique in that the IO cell presents its differential amplifier inputs and outputs to the device pins for external use only. There are no signals from the core of the device involved. This setting is used for the creation of an output smoothing filter for a differential analog signal sourced by another IO site.

VMR Output

The VMR Output setting places the device's internal signal reference (1.5 V) on two pins of the IO site.

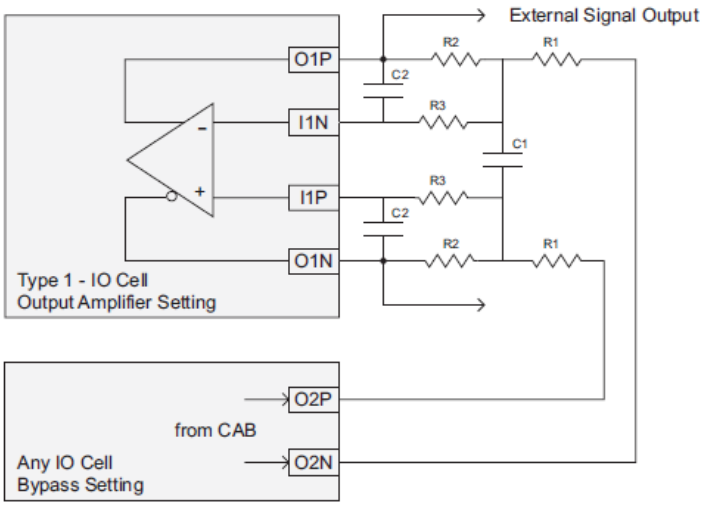
Amplifier Detail - Rauch Filter Designs

The Amplifier setting of the Type 1 and 1a IO cells accommodates construction of continuous time input anti-aliasing and output smoothing filters. Rauch (a.k.a. multiple feedback, MFB) differential filter construction is the recommended topology.



Rauch Input Anti-Aliasing Filter

The same filter design technique can also be used in the construction of an output smoothing or recon- struction filter. In this case, the unfiltered output signal is sourced by a Bypass output and the amplifier used to construct the filter is provided by an adjacent IO cell using its output Amplifier setting.



Rauch Output Smoothing Filter

Types 2 and 2a IO Cells

The device contains two Type 2 and one Type 2a IO cells. These IO sites provide additional flexibility for getting signals in and out of the CABs. Type 2 and 2a IO cell options are summarized below:

- Bypass I/O
  - Differential Input
  - Differential Output
- Digital Input
  - Single Ended Input (two per IO Cell) Digital Output
  - Single Ended Output (two perIO Cell)
    - Chip Clock
    - Comparator
    - RAM Transfer Done
- Analog Input
  - Low Offset Chopper Amplifier (type 2a IO cell only) VMR Output
  - Internal signal reference (1.5 V) presented on both pins.

Digital Input

Two independent single ended logic control signals can be routed into the CAMs.

Digital Output

The Type 2 and 2a IO cells can be configured to provide two singled ended digital outputs. The outputs can reflect: any of the 6 internal clocks, a comparator or ADC-SAR output or a signal indicating the completion of a transfer from Shadow SRAM to Configuration SRAM. The polarity of these output signals is programmable.

Analog Input

Like the Type 1a IO cell, the Type 2a IO cell also offers a Low Offset Chopper Amplifier. The 2a Chopper Amplifier has programmable gain ranging from 0 up to 60 dB in 10 dB steps.

SRAM

There are three regions of volatile SRAM within the device. The first, Shadow SRAM, is the memory that gets written to during configuration or reconfiguration. Shadow SRAM serves as a temporary holding area for configuration data prior to its transfer into Configuration SRAM. This second region, Configuration SRAM, controls the behavior of the analog signal processing circuitry. The transfer from Shadow SRAM to Configuration SRAM happens in a single clock cycle, minimizing disturbance to the analog signal paths. The third region of memory is the Look-Up Table.

LUT

The device contains a Look-Up Table (LUT) memory. The LUT provides replacement values for Configuration SRAM locations. A CAB plus LUT combination can be used to create non-linear functions such as arbitrary waveform synthesis and table based sensor linearization functions.

Auxiliary Cell

Recall that the device contains both Shadow SRAM and Configuration SRAM. Configuration SRAM controls the behavior of the analog signal processing elements. Data written into the device, loads into Shadow SRAM and remains there until an internal signal enables the transfer to Configuration SRAM.

At the end of a Primary Configuration, the transfer takes place only when the Activate pin pulls high.

Once a Primary Configuration has completed, an AN23x device can accept subsequent reconfiguration data into its Shadow SRAM (see section 5.1.4 for further details on the Update protocol). The timing of the transfer of reconfiguration data from Shadow SRAM to Configuration SRAM can be tightly controlled using one of several methods made available via the RAM Transfer Cell:

Immediate

The Immediate setting of the RAM Transfer Cell forces the reconfiguration data to transfer into the Configuration SRAM as soon as the external write of the reconfiguration data completes.

Event Driven

The Event Driven setting of the RAM Transfer Cell allows the use of either an internal or external digital control signal to cause the transfer of data to occur. Internal event signals are typically sourced by a comparator output.

Event Driven and Armed

An arming term is available to hold off the Event Driven trigger of data transfer. When using the arming function, either the Trigger or Arm terms may be sourced externally, but not both.

Clock Synchronization

The Clock Synchronization setting forces the SRAM transfer to occur only at the point at which all chip clocks have a simultaneous rising edge. This ensures that clock synchronization is maintained when making changes to clock dividers, but will cause a delay between the end of the reconfiguration bit-stream and the transfer.

Reconfiguration

The most powerful use model of Okika Technologies FPAAs includes the use of a companion host processor. The FPAA is used with MODE tied low and consequently the configuration interface presents itself as a SPI compatible Slave. The host processor can be used to simply manage the configuration tasks, downloading data to the FPAAs from its SPI Master port. The real potential of programmable analog however is best leveraged when the host processor is also used to generate and download new configuration data sets on-the-fly as analog signal processing requirements change. Please refer to Okika Technologies Dyamx Design Lab help manuals to get more information on “C Code Generation” and this powerful application approach. This data sheet focuses only on the physical requirements of the interface between a host processor and the FPAA.

1. Configuration Data Stream Protocol

Regardless of whether the FPAA is being applied in either the Master or Slave modes, the serial configuration data stream adheres to an Okika Technologies proprietary protocol. Okika Technologies Dynamx Design Lab constructs a configuration data file compliant to this protocol so that even for the simplest case of self-booting from a slaved SPI PROM, all of the requisite information is contained in the data stream delivered to the device.

In dynamic applications, multiple configuration data files may be generated by Dynamx Design Lab and stored as an array of configurations on the host processor. For example, if there are three filter configurations required the host system may store the associated configuration data file as Filter1, Filter2, and Filter3, each an element of the configuration system. Then host software may reconfigure the OTC24000 into any of the filters at any time.

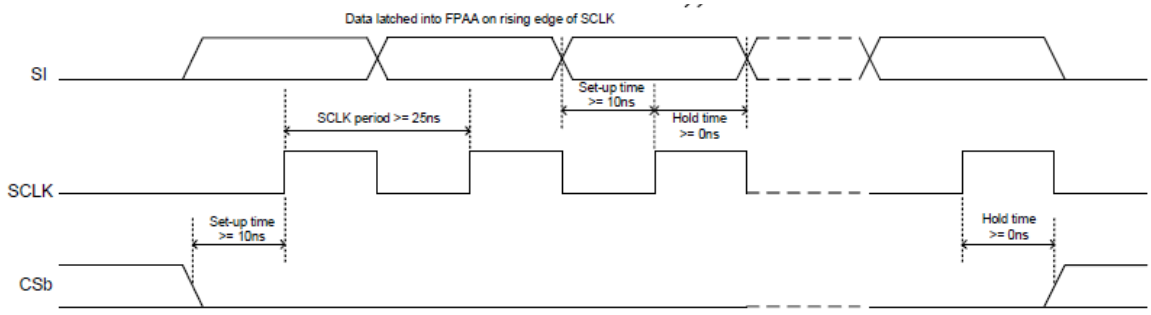
Alternatively, most analog modules in the Dynamx Design Lab library include C-code generation that enables host processing to automatically generate the configuration data file. For example, if a filter is required that can be programmed to arbitrary response, gain, or quality values, C-code routines that take F0, G, and Q as inputs are available. When called by host firmware these routines output a complete configuration file, ready to load into OTC24000 via the SPI interface after appropriate headers and footers are added to be in compliance with the Okika protocol. For more information on the protocol and how to construct a complete configuration data file please contact Okika Technologies.

Important Note:

The Okika Technologies OTC24000 device is a complex configurable analog circuit that is intended to be used in conjunction with our Dynamx Design Lab design and simulation software. That software fully automates the process of designing and configuring the OTC24000 as well as generating configuration data files and C code for user host controller applications. Okika does not recommend and does not support users attempting to generate data files outside of the Dynamx Design Lab environment without support. The Dynamx Design Lab environment includes an extensive library of Configurable Analog Modules that may be used in the schematic editor and simulator to build complex circuits. The user can then focus on system requirements, design, quick-prototyping, and design verification and then leave the complexities of configuration data generation and management to the Okika software tools. For more information visit the Okika Technologies download site to access the latest version of design support software.

Configuration Interface Timing

Timing for the OTC24000 SPI interface is shown in the diagram below.



Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies [a]	AVDD BVDD DVDD	-0.5	-	3.6 V	V	AVSS, BVSS and DVSS all held to 0.0 V
xVDD to yVDD Offset		-0.5		0.5	V	Ideally all supplies should be at the same voltage
Package Power Dissipation,	Pmax 25°C Pmax 85°C	-	-	4.5 1.8	W	(Theoretical values based on Tj=125deg.C) Still air, No heatsink, 44 pads and exposed die pad soldered to PCB θja = 22.5°C/W. VDD = 3.3V
AN231E04 max power dissipation	dpASPmax	-	-	0.25	W	Maximum power dissipation all resources used, (see section 1.5.13 for more detail).
Input Voltage	Vinmax	VSS-0.5	-	VDD+0.5	V	
Ambient Operating Temperature	Top	-40	-	85	°C	
Storage Temperature	Tstg	-40		125	°C	

[a] Absolute Maximum DC Power Supply Rating - The failure mode is non-catastrophic for VDD of up to 5 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related issues.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	AVDD BVDD DVDD	3.0	3.3	3.6	V	AVSS, BVSS and DVSS all held to 0 V
Analog Input Voltage.	Vina	VMR -1.375	-	VMR +1.375	V	Conditional on the circuit which is being driven. This limit is defined as maximum signal amplitude through input Sample and hold cell which results in >-80dB THD+N using a 1KHz test signal. VMR is 1.5 volts above AVSS
Digital Input Voltage	Vind	0	-	DVDD	V	
Junction Temp [b]	Tj	-40	-	125	°C	Assume a package θja=22.5°C/W

[b] To calculate the junction temperature (Tj) you must first empirically determine the current draw (total Idd) for the design. The programmable nature of this device means this can vary by orders of magnitude between different circuit designs. Once the current consumption is established then the following formula can be used; Tj = Ta + Idd x VDD x 22.5 °C/W, where Ta is the ambient temperature. Worst case θja = 22.5 °C/W assumes no air flow and no additional heatsink, 44 pads and the exposed die pad soldered to PCB.

General Digital I/O Characteristics (VDD = 3.3v +/- 10%, -40 to 85 deg.C)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low	Vih	0	-	30	-	% of DVDD
Input Voltage High	Vil	70	-	100	-	% of DVDD
Output Voltage Low	Vol	0	-	20	-	% of DVDD
Output Voltage High	Voh	80	-	100	-	% of DVDD
Input Leakage Current	Iil	-	-	+/-1	µA	Some pins have active pull up/ down, please see below.
Max. Capacitive Load	Cmax	-	-	10	pF	
Min. Resistive Load	Rmin	50	-	-	Kohm	Each pins has a specific load driving capability, detailed in sections 1.4 and 1.5
ACLK Frequency	Fmax	-	16	40	MHz	Divide down to <4 MHz prior to use as a CAB clock
Clock Duty Cycle	CLKduty	45	-	55	%	All clocks

Digital I/O Characteristics (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

Pins ACLK, SCLK, RESETb, CS1b, CS2b, SI, MODE (standard CMOS inputs)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low	Vil	0	-	30	%	% of DVDD
Input Voltage High	Vih	70	-	100	%	% of DVDD

Pin SO, (standard CMOS output)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Voltage Low	Vol	VSS	-	VSS	mV	Load 10pF//50Kohm to VSS
Output Voltage High	Voh	3.28	-	VDD	V	Load 10pF//50Kohm to VSS VDD = 3.3 V.
Max. Capacitive Load	Cmax	-	-	100	pF	Maximum load 100 pF // 5 Kohm at up to 5MHz.
Min. Resistive Load	Rmin	5	-	-	Kohm	Maximum load 100 pF // 5 Kohm at up to 5MHz.
Current Sink	Isnkmax	60	100	135	mA	Pin shorted to VDD Current should be limited externally so that it does not exceed 3mA
Current Source	Isrcmax	50	80	110	mA	Pin shorted to VSS. Current should be limited externally so that it does not exceed 3mA

Digital functions of mixed signal Pins IO1, IO2, IO3, IO4, IO5, IO6, IO7,

These pins can be configured by the user to be standard CMOS input or outputs.
I/O cells 5, 6 and 7 the pin pairs can be connected to and used individually.
I/O cells 1 through 4 provide pin pairs for differential (complimentary) digital connections.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low	Vil	0		30	%	% of DVDD
Input Voltage High	Vih	70		100	%	% of DVDD
Output Voltage Low	Vol	VSS	-	VSS	mV	Pin load = 20pF//10K to VSS
Output Voltage High	Voh	3.25	-	VDD	V	Pin load = 20pF//10K to VSS VDD = 3.3 V.
Max. Capacitive Load	Cmax	-	-	50	pF	Maximum load 20 pF // 10 Kohm at up to 4MHz signal
Min. Resistive Load	Rmin	50	-	-	Kohm	Maximum load 20 pF // 10 Kohm at up to 4MHz signal
Current Sink	Isnkmax	15	30	40	mA	Pin shorted to VDD. Current should be limited externally so that it does not exceed 3mA
Current Source	Isrcmax	15	25	35	mA	Pin shorted to VSS. Current should be limited externally so that it does not exceed 3mA.

Pins ERRb (Open Drain, CMOS transistor)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low	Vil	0		30	%	% of DVDD,
Input Voltage High	Vih	70		100	%	% of DVDD
Output Voltage Low	Vol	VSS	-	7.0	mV	10KOhm to VDD VDD = 3.3 V.
Output Voltage High	Voh	3.29	-	VDD	V	10KOhm to VDD VDD = 3.3 V.
Max. Capacitive Load	Cmax	-	-	10	pF	Maximum load 10 pF // 50 Kohm at full BW
Min. Resistive Load	Rmin	50	-	-	Kohm	Maximum load 10 pF // 50 Kohm at full BW
Current Sink	Isnkmax	50	-	110	mA	Pin shorted to VDD. Current should be limited externally so that it does not exceed 3mA
Current Source	Isrcmax	-	-	+/-1	µA	Pin shorted to VSS
External Resistive Pullup	Rpullupext	10	10	10	Kohm	MUST be used

Pins ACTIVATE, CFGFLGb

These pins are Open Drain CMOS transistors, with optional user configurable internal pull-up resistor
We also note that the output voltage on these pins is “sensed” by internal circuitry, (see figure 2 below)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low	Vil	0		30	%	% of DVDD
Input Voltage High	Vih	70		100	%	% of DVDD
Output Voltage Low	Vol	80	-	140	mV	Pin load = Internal pullup + external 10pF//50K to VSS VDD = 3.3 V.
Output Voltage High, internal pull-up.	Voh	3.05	-	3.16	V	Pin load = Internal pullup + external 10pF//50K to VSS VDD = 3.3 V.
Output Voltage Low, external pull-up.	VolE	529	-	773	mV	Pin load = 5K to VSS VDD = 3.3 V.
Output Voltage High	Voh	VDD	-	VDD	V	Pin load = 5K + 10pF to VSS
Max. Capacitive Load	Cmax	-	-	10	pF	Maximum load 10 pF // 50 Kohm at full BW
Min. Resistive Load	Rmin	50	-	-	Kohm	Maximum load 10 pF // 50 Kohm at full BW
Current Sink, pull down only	Isnkmax	1.8	-	3.7	mA	Pin shorted to VDD.
Current Source, pull up only	Isrcmax	0.34	-	1.1	mA	Pin shorted to VSS.
Internal Resistive Pullup	Rpullupint	3.5	5.3	8.4	Kohm	Default, not used with external pullup.

External Resistive Pullup	Rpullupext	5	7.5	10	Kohm	Optional - to be used only if internal pullup is deselected

Pin LCCb/DOUT1 (CMOS Output)

The primary function of this pin is as LCCb (Local Configuration Complete), this signal is used in multiple dpASP designs to pass Chips Select from dpASP to dpASP enabling primary configuration of a serial chain of dpASP's from a single SPI bus, please refer to the AN231E04 User Guide for details.
If the LCCb signal pin is not required (e.g. a circuit design with a single dpASP device) then via dpASP configuration this pin can be used as a digital output, this is realized by adjusting the properties of the dpASP "digital I/O cell".

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Voltage Low, (LCCb)	Vol(LCCb)	VSS	-	VSS	mV	Load 10pF//50Kohm to VSS, during configuration.
Output Voltage High, (LCCb)	Voh(LCCb)	3.00	-	3.20	V	Load 10pF//50Kohm to VSS, during configuration. VDD = 3.3 V
Output Voltage Low, (DOUT1)	Vol(DOUT1)	VSS	-	VSS	mV	Load 10pF//50Kohm to VSS, When configured to pin39=DOUT1
Output Voltage High, (DOUT1)	Voh(DOUT1)	3.29	-	VDD	V	Load 10pF//50Kohm to VSS, When configured to pin39=DOUT1 VDD = 3.3 V.
Max. Capacitive Load	Cmax	-	-	10	pF	Maximum load 10 pF // 50 Kohm
Min. Resistive Load	Rmin	50	-	-	Kohm	Maximum load 10 pF // 50 Kohm
Current Sink, (LCCb)	Isnk(LCCb)	3.0	-	7.0	mA	LCCb (pin 39) shorted to VDD, during configuration. Current should be limited externally so that it does not exceed 3mA.
Current Source, (LCCb)	Isrc(LCCb)	0.25	-	0.80	mA	LCCb (pin 39) shorted to VSS, during configuration.
Current Sink, (DOUT1)	Isnk(DOUT1)	20.0	-	60.0	mA	DOUT1 (pin 39) shorted to VDD,. Current should be limited externally so that it does not exceed 3mA.
Current Source, (DOUT1)	Isrc(DOUT1)	12.5	-	35.0	mA	DOUT1 (pin 39) shorted to VSS, Current should be limited externally so that it does not exceed 3mA.
Clock skew (DOUT1 connected to "clocka")	CLK_{SKEW}	-	8.0	-	ns	Skew at DOUT1 (pin 39) relative to external signal clock applied to input pin ACLK (pin 34). Note; This is only valid when DOUT1 is selected to output the CAM clockA, and CAM clockA is derived from ACLK divided by1.
Comparator skew (DOUT1 connected to "comparator")	$COMP_{SKEW}$	-	25.0	-	ns	This is the delay of the comparator CAM output transition relative to the exported comparator clock clock appears on the output pin. Note, The comparator is clocked with a user programmable CAM clock derived from a division of ACLK
RAM transfer delay (DOUT1 connected to "RAM transfer Pulse")	RAM_{DELAY}	-	20.0	-	ns	This is the delay of the signal at the dpASP pin 39, (DOUT1) relative to the actual internal transfer event.

Auto-null/Osc start delay (DOUT1 connected to “Auto-null/Osc start done” signal)	$DONE_{DELAY}$	-	40	-	ms	This is the delay of the signal at the dpASP pin 39, (DOUT1) relative to the actual internal event.

Digital I/O Characteristics, continued (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

MEMCLK/DOUT2 (CMOS Output)

The primary function of this pin is as MEMCLK (Memory Clock), this signal is used as a clock output in circuit designs which require configuration from an SPI PROM (or SPI EEPROM), please refer to the AN231E04 User Guide for details.
If the MEMCLK signal pin is not required (e.g. a circuit configured from a microcontroller) then via dpASP configuration this pin can be used as a digital output.
The MEMCLK signal is only active when the dpASP MODE (pin35) is high (tied to VDD).
DOUT2 function cannot be used if dpASP MODE (pin35) is high (tied to VDD).

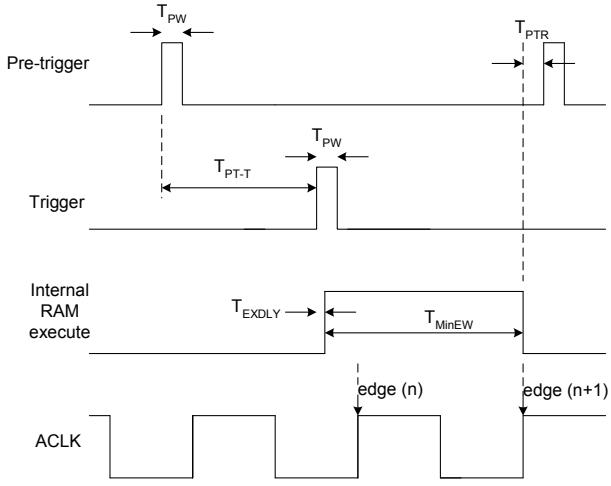
Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Voltage Low, (MODE pin 35 = VSS, DOUT2 inactive)	Vol	VSS	-	VSS	mV	Load 10pF//50Kohm to VSS. This Pin MEMCLK is unused in this MODE=VSS, there is an internal weak pull down resistor
Output Voltage Low, (MODE pin 35 = VSS, DOUT2 active)	Vol	VSS	-	VSS	mV	Load 100pF//5Kohm to VSS
Output Voltage Low, (MODE pin 35 = VDD)	Vol	VSS	-	VSS	mV	Load 100pF//5Kohm to VSS
Output Voltage High	Voh	3.28	-	VDD	V	Load 100pF//5Kohm to VSS, VDD = 3.3V.
Max. Capacitive Load	Cmax	-	-	100	pF	Maximum load 100 pF // 5 Kohm
Min. Resistive Load	Rmin	5	-	-	Kohm	Maximum load 100 pF // 5 Kohm
Current Sink, (MODE pin 35 = VSS & DOUT2 inactive)	Isnk	0.01	0.03	0.05	mA	Pin shorted to VDD. Th This Pin MEMCLK is unused when MODE=VSS and DOUT2 is inactive. Thus No active drive.
Current Source, (MODE pin 35 = VSS & DOUT2 inactive)	Isrc	-	-	+/-1	uA	Pin shorted to VSS. This Pin MEMCLK is unused when MODE=VSS and DOUT2 is inactive. Thus No active drive.
Current Sink, (MODE pin 35 = VDD or DOUT2 active)	Isnk	60	100	135	mA	Pin shorted to VDD. Current should be limited externally so that it does not exceed 3mA
Current Source, (MODE pin 35 = VDD or DOUT2 active)	Isrc	50	80	110	mA	Pin shorted to VSS. Current should be limited externally so that it does not exceed 3mA
Clock skew (DOUT2 connected to “clocka”)	CLK_{SKEW}	-	8.0	-	ns	Skew at DOUT2 (pin 42) relative to external signal clock applied to input pin ACLK (pin 34). Note; This is only valid when DOUT2 is selected to output the CAM clockA, and CAM clockA is derived from ACLK divided by1.

Comparator skew (DOUT2 connected to “comparitor”)	$COMP_{SKEW}$	-	25.0	-	ns	This is the delay of the comparator CAM output transition relative to the exported comparator clock clock appears on the output pin. Note, The comparator is clocked with a user programmable CAM clock derived from a division of ACLK
RAM transfer delay (DOUT2 connected to “RAM transfer Pulse”)	RAM_{DELAY}	-	20.0	-	ns	This is the delay of the signal at the dpASP pin 42, (DOUT2) relative to the actual internal transfer event.
Auto-null/Osc start delay (DOUT2 connected to “Auto-null/Osc start done” signal)	$DONE_{DELAY}$	-	40	-	ms	This is the delay of the signal at the dpASP pin 42, (DOUT2) relative to the actual internal event.

RAM Transfer – Trigger and Arm

These digital inputs do not have dedicated pins, a connection exists within the dpASP, an external signal can be routed to either of these virtual pins from a type2 I/O cell (I/O cells 5, 6 and 7. Pins 15,16,17,18,19 or 20).
The purpose of these virtual pins is to extend optional asynchronous timing control of the dpASP configuration to the user.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low	Vil	0		30	%	% of DVDD
Input Voltage High	Vih	70		100	%	% of DVDD
Minimum pulse width connected to where	T_{PW} setup time	5	-	-	ns	Time to register the event internally.
Pulse-Pulse edge delay	T_{PT-T} setup time	10	-	-	ns	Delay between pre-trigger and trigger. Need not be observed if pre-trigger is not used, is set at the end of configuration automatically.
Execute delay	T_{EXDLY}	0	10	20	ns	Delay from trigger rising edge to internal execute event.
Execute minimum width	T_{MinEW}	1 ALCK	-	2 ACLK	-	Duration of execute pulse guaranteed 1 ACLK period. Can be as long as 2 periods depending on relative phases.
Pre-trigger reset.	T_{PTR}	10	-	-	ns	Pre-trigger circuit is reset ready to accept another pre-trigger.



AnadigmDesigner2 options, (these are set using the software tool AnadigmDesigner2)

RAM Transfer Trigger = Automatic :

RAM transfer happens automatically immediately after the “end” byte of a configuration bit stream. Timing control is entirely inside the AN231E04 device and not visible to a user.

RAM Transfer Trigger = Event driven.

RAM Trigger = Off.

no pre-trigger used. The “end” byte of configuration bit stream arms the RAM transfer and the user signal then acts as the trigger.

Arm Trigger = On

External Signal Allowed = Trigger. This setting allows the external signal connected to be the trigger, Arming must be from an internal signal.

External Signal Allowed = Arm. This setting allows the external signal connected to be the arming signal, Trigger be from an internal signal.

RAM Transfer Trigger = Clock synch

RAM transfer happens automatically immediately following the first occurrence of all internal clocks being scyncronous. Timing control is entirely inside the AN231E04 device and not visible to a user.

HINT: The RAM transfer timings above are for the trigger block hardware - The **Trigger** and **Arm** signals can come from many sources, propagation delays to the trigger block inputs will vary depending on the source and routing of the signals to this block.

Analog I/O Characteristics (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

Analog Inputs General

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Range	Vina	VMR - 1.375	-	VMR + 1.375	V	VMR set to 1.5V
Differential Input	Vdiffina	0	-	+/-2.75	V	VMR = 1.5 V.
Common Mode Input Range	Vcm	1.4	1.5	1.6	V	Limited by signal clipping for large waveforms. Please see figures
Input Offset	VosIOInt	-	3.0	18	mV	IO cell, unity gain mode intrinsic
	VosIOAZ	-	0.5	1.0	mV	IO cell, unity gain mode, auto-null on.
	VosCabI	-	3	18	mV	CAB, unity gain mode.
	VosCabAz	-	250	1000	uV	CAB, unity gain mode, auto-null on.
	VosCabzC	-	75	250	uV	CAB, unity gain mode, auto-null and chopping on.
Input Frequency	Fain	0	<2	8	MHz	Max value is clock, CAM and input stage dependent. Input frequency for most CAMs is limited to approx <2MHz due to CAM signal processing which is based on sampled data architectures.

Differential Operational Amplifier

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output voltage range	Vinouta	VMR - 1.375	-	VMR+ 1.375	V	VMR = 1.5V. Measured for IO SnH circuit.
Differential Input/Output	Vdiffioa	-	-	+/-2.75	V	Common mode voltage = 1.5 V. Measured for IO SnH circuit.
Common Mode Input Voltage Range (Note1)	Vcm	VMR	VMR	VMR	V	Limited due to causing signal clipping for large waveforms. VMR can be varied if supplied externally (+200mV to -1.0volt)
Common Mode Output Voltage Deviation from VMR	Vcm	-	23.5	72.7	mV	Due to common mode offsets.
Equivalent Input Voltage Offset.	VoffsetI	-	3.0	18.0	mV	Intrinsic offset voltage.
Equivalent Input Voltage Offset.	VoffsetAZ	-	500	1000	uV	Auto-null offset voltage, rectangular distribution.
Auto-null time, from LCCb falling edge.	T_{AZ}	-	60	-	ms	see application note AN231002 “Auto-nulling within the AN231E04”
Offset Voltage Temperature Coefficient	VoffsettAZTC	-	4	-	µV/°C	Auto-null mode, from -40°C to 125°C.
Power Supply Rejection Ratio	PSSR	60	-	-	dB	Sample and Hold mode, 1MHz clk, at DC
Common Mode Rejection Ratio	CMRR	60	-	-	dB	Sample and Hold mode, 1MHz clk, at DC

Differential Slew Rate	Slew	-	50	-	V/µsec	Opamp driving off chip with Max load. Effective internal slew is affected by the internal routing and load is normally much faster
Unity Gain Bandwidth.	UGB	-	63	-	MHz	10pF external load
Open loop gain	Av	-	103	-	dB	
Input Impedance	Rin	10	-	-	Mohm	Voltage gain mode
Output Impedance	Rout	-	33	-	Ohms	Measured at package pins. Track impedance increases the effective output impedance. The OpAmp is designed to drive all internal nodes,
Output Load, External	Rload	1	-	-	Kohm	
Output Load, External	Cload	-	-	100	pF	
Noise Figure	NF	-	0.16	-	µV/√Hz	Unity gain mode.
Signal-To Noise Ratio and Distortion	SINAD	-	97	-	dB	Unity gain mode.
Spurious Free Dynamic Range	SFDR	-	96	-	dB	Unity gain mode.

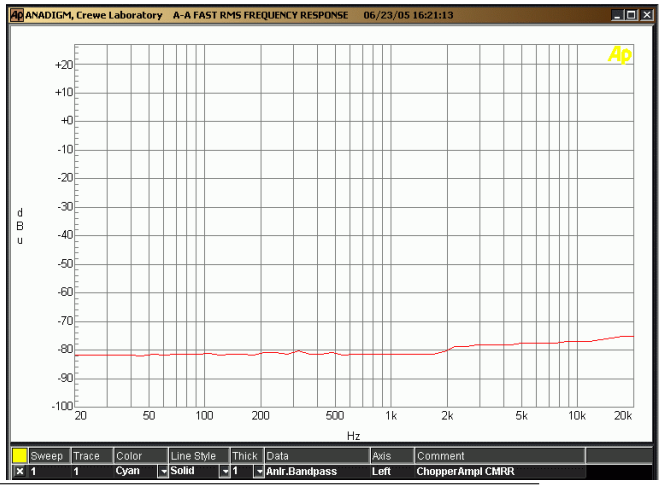
Cell, Sample and Hold Mode

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Range	Vina Vdiffina	See analog input above				
Equivalent Input Offset Voltage	VosI	-	3	18	mV	Non auto-null differential opamp offset
	VosAZ	-	500	1000	uV	Auto-null differential opamp offset[3]
Offset Voltage Temperature Coefficient	VoffsettcAZ	-	4	-	µV/°C	With auto-null active. From -40°C to 125°C
Input Frequency	Fain	0	-	2	MHz	Generally limited by aliasing to half Sample and Hold clock.
Power Supply Rejection Ratio	PSRR	60	-	-	dB	d.c.
Common Mode Rejection Ratio	CMRR	60	-	-	dB	
Input Resistance	Rin	10		-	Mohm	R=1/Cf equivalent
Input Capacitance	Cin	-		8.0	pF	Switched capacitances
Input Referred Noise Figure	NF	-	0.16	-	µV/√Hz	0dBu input, 1KHz, Noise summed from 20Hz to 22KHz
Signal-to Noise Ratio and Distortion	SINAD	-	84	-	dB	0dBu input, 1KHz, Noise summed from 20Hz to 22KHz
Spurious Free Dynamic Range	SFDR	-	90	-	dB	0dBu input, 1KHz

Chopper Amplifier Cell

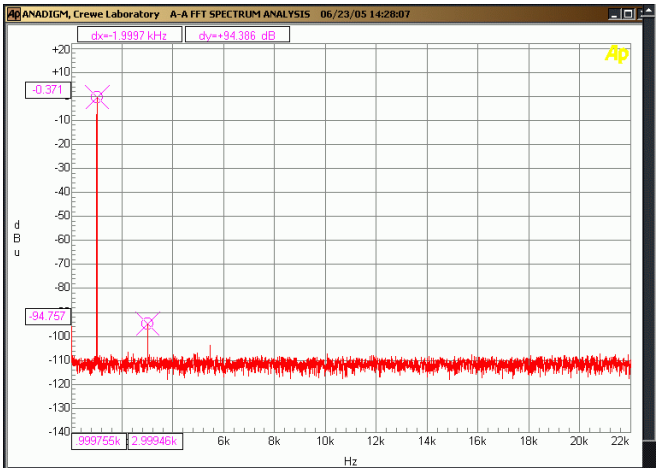
Parameter	Symbol	Min	Typ	Max	Unit	Comment

Input Range	Vina Vdiffina	See analog input above			-	Usable input range will be reduced by the effective gain setting
Gain	Ginamp	0dB	-	60dB	-	Software selected
Gain Accuracy	GA 0dB	-	-	5	%	0dB setting, 1KHz test signal.
	GA10dB		-	5	%	10dB setting, 1KHz test signal.
	GA20dB		-	5	%	20dB setting, 1KHz test signal.
	GA30dB		-	5	%	30dB setting, 1KHz test signal.
	GA40dB		-	5	%	40dB setting, 1KHz test signal.
Equivalent Input Offset Voltage	VosI	-	0.5	14	mV	Intrinsic differential opamp offset
Equivalent Input Offset Voltage	VosAZ1	-	250	500	uV	Differential opamp offset, auto-nulled, NOT chopped.
Equivalent Input Offset Voltage	VosAZ2	-	25	100	uV	Differential opamp offset, auto-nulled and chopped.
Offset Voltage Temperature Coefficient	VoffsettcAZ	-	15	TBD	µV/°C	With auto-null and chopping active. From -40°C to 125°C
Input Frequency	Fain	0	-	-	KHz	Generally 10x slower than clock, application dependent.
Power Supply Rejection Ratio	PSRR	-	62	-	dB	DC. Amp Gain = 0dB
Common Mode Rejection Ratio	CMRR	-	81	-	dB	250kHz clock, 1kHz 0dBu output. See figure 1
Large Signal Harmonic Distortion	Dist	-	-77	-	dB	Unity-gain. 0dBu input at 1KHz
Input Resistance	Rin	10		-	Mohm	
Input Capacitance	Cin	-		5.0	pF	
Input Referred Noise Floor	IRN	-	20	-	nV/√Hz	20dB-gain, 250kHz clock. IIdle channel.
Input Referred Noise Floor	IRN	-	4	-	nV/√Hz	60dB-gain, 250kHz clock. IIdle channel.
Signal-to Noise and Distortion Ratio	SINAD	-	76	-	dB	20dB-gain, 250kHz clock. 0dBu output at 1KHz. Noise and distortion summed from 22Hz to 22KHz
Spurious Free Dynamic Range	SFDR	-	90	-	dB	20dB-gain, 250kHz clock. 0dBu output at 1KHz, See figure 2



1.

Figure 1: ChopperAmplifier CMRR



2.

Figure 2: ChopperAmplifier SFDR

Analog Outputs, Loading & Signal Conditioning

(The IO cells use the same circuits as the input cells)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Min load R	RloadMin	1	-	-	KOhm	to VSS
Rout	R_{OUTIO}	-	33	-	Ohms	For IO opamp to package pins.
	R_{OUTCAB}	-	530	-	Ohms	For CAB opamp to package pins, (depends on CAB and IO used) Core to outside in bypass I/O.
Max load C	Cload Max	-	-	100	pF	to VSS.
Large signal swing	SIG_{LARGE}	VMR-1.375	-	VMR+1.375	V	Differential voltage where -80dB THD is reached for IO cell in SnH mode. 10pF load.
Common Mode Voltage	Vcm	-	VMR	-	V	Derived from on chip VMR voltage.
Common Mode Voltage Deviation	VcmDV	-	-	-	mV	Deviation from supplied VMR. Values are quoted for IO cell or CAB opamp. See other tables.

Clock Dividers

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Division ratio Primary divider	$DIV_{RATIOPR}$	1	-	510	-	Software controlled.
Division ratio secondary divider	$DIV_{RATIOSEC}$	1	-	510	-	Software controlled.
Division ratio auto zero clock	DIV_{AZ}	1000	162K	510K	-	Typical is default value.
Min clock speed	CLK_{MIN}	-	1kHz @ 25°C) 10kHz @ 85°C	-	KHz	Each CAM has a different lower clock frequency depending on the parameters set. Excessively low clock frequency will cause signal droop.
Max clock speed	CLK_{MAX}	-	-	8	MHz	Each CAM has a different upper clock frequency depending on the parameters set. Excessively high clock frequency will cause poor settling and loss of precision.
Phase delay	$Phase_D$	0	-	255	cycles	Measured in terms of cycles of clock from a primary clock divider.

PORb & Auto-null

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Intrinsic Porb duration	$Porb_{DEL}$	0.5	1	2	ms	After release of Porb pin.
Porb brown out voltage	$Porb_{BROWN}$	0.8	1.1	1.5	V	Porb will reset device if VDD drops below this level to prevent RAM corruption.
Auto-null period	AZ_{DEL}	-	60	-	ms	Duration for AZ cycle of opamps

VMR (voltage Mid Rail) and VREF (Reference Voltage) Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VMR Output Voltage	Vvmr	1491	1500	1509	mV	At 25°C, VDD=3.3 volts, see figure 3
VREF+ Output Voltage	Vref+	2469	2492	2515	mV	At 25°C, VDD=3.3 volts, see figure 4
VREF- Output Voltage	Vref-	481	501	520	mV	At 25°C, VDD=3.3 volts, see figure 4
Output Voltage Deviation VMR	Vrefout	-	0.5	1.0	%	Over process and supply voltage corners
Output Voltage Deviation VREF+, VREF-	Vrefout	-	1.0	2.0	%	Over process and supply voltage corners
Voltage Temperature Coefficient VREF+, VMR, VREF-	Vreftc	-	-	-	-	See typical graphical data below -40°C to 125°C
Power Supply Rejection Ratio, VMR	PSSR	TBD	-	-	dB	DC

Power Supply Rejection Ratio Vref + and Vref-	PSSR	TBD	-	-	dB	DC
Start Up Time	Tstart	-	-	1	ms	Assuming recommended capacitors, 25°C, VDD=3.3 volts

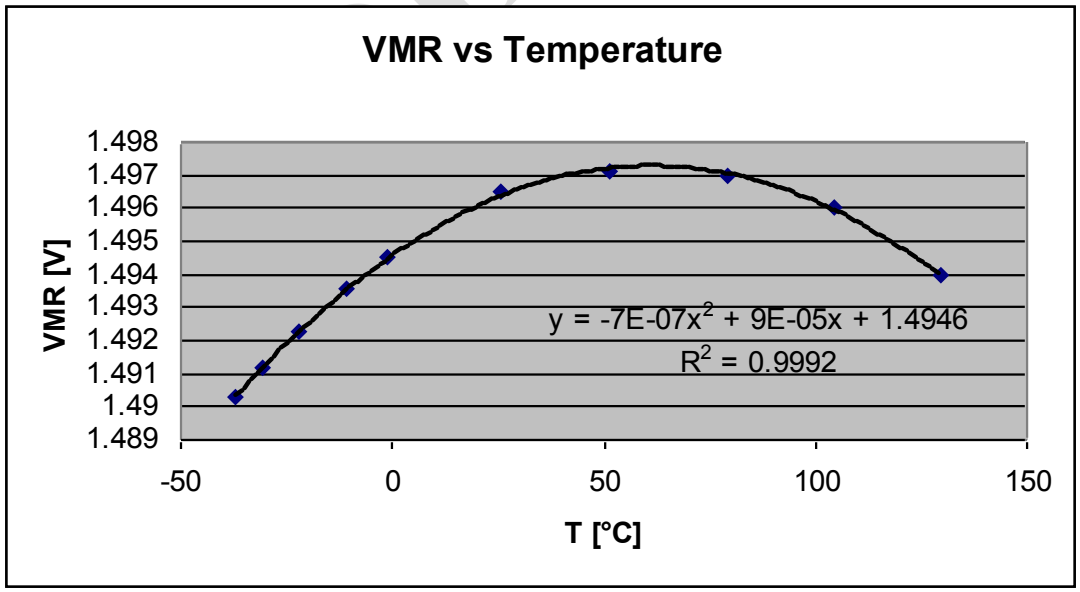


Figure 3: GainHold CMRR

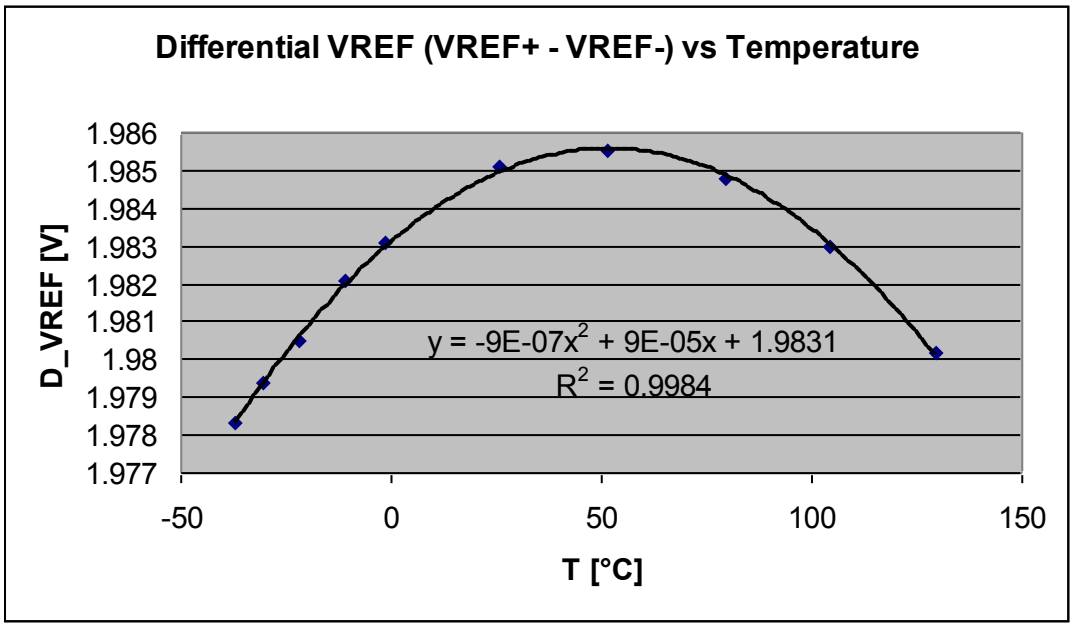


Figure 4: GainHold CMRR

CAB (Configurable Analog Block) Differential Operational Amplifier

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Range	Vinouta	0.05	-	2.95	V	GainInv 1kHz THD > -80dB. Common mode voltage = 1.5 V
Differential Output voltage	Vdiffioa	-	-	+/-2.9	V	Limited by signal clipping. GainInv THD exceeds -80dB Common mode voltage = 1.5 V
Common Mode Input Voltage Range	Vcm	1.4	1.5	1.6	V	VMR set to 1.5V
Common Mode Voltage Deviation	VcmD	0	-	+/-50	mV	Deviation is caused by opamp common mode offset voltages.
Equivalent Input Voltage Offset.	VoffsetI	-	3	18	mV	Intrinsic offset voltage.
Equivalent Input Voltage Offset.	VosAZ	-	250	1000	uV	Auto-null offset voltage.
Equivalent Input Voltage Offset.	VosAZchpI	-	75	250	uV	Auto-null & chopped offset
Offset Voltage Temperature Coefficient	VosAZ	-	see graph	19	µV/°C	Auto-null mode, from -40°C to 125°C.
Offset Voltage Temperature Coefficient	VosAZChp	-	-	< 0.1	µV/°C	Auto-null and chopped mode, from -40°C to 125°C.
Power Supply Rejection Ratio	PSSR	-	60	-	dB	DC. Variation between CAMs is expected because of variations in architecture.
Common Mode Rejection Ratio	CMRR	-	54	-	dB	GainInv CAM, clock = 1MHz, gain = 1. -20dBu input at 1kHz See figure 6
Differential Slew Rate, Internal	SlewI	-	35	-	V/µsec	Applicable when the OpAmp load is internal to the dpASP
Differential Slew Rate, External	SlewE	-	30	-	V/µsec	Applicable when the OpAmp driving signal out of the dpASP package. Routing resistance causes degradation from Slew
Unity Gain Bandwidth, Full Power Mode.	UGB	-	18	-	MHz	Applicable when sourcing and loading the OpAmp with a load internal to the dpASP. CAMs limit signal frequency to a lower value. See figure 5
Input Impedance, Internal	Rin	10	-	-	Mohm	
Output Impedance, Internal	Rout	-	-	-	Ohms	The OpAmp output is designed to drive all internal nodes, these are dominantly capacitive loads
Output Impedance, External	Rout	-	600	-	Ohms	Output to a dpASP output pin (output cell bypass mode). This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture
Output Load, External	Rload	1	-	-	Kohm	
Output Load, External	Cload	-	-	100	pF	
Input Referred Noise Floor	IRN	-	300	-	nV/√Hz	Unity-gain GainHold CAM, 1MHz clocking. Idle channel.
Signal-To Noise and Distortion Ratio [8]	SINAD	-	86	-	dB	Unity-gain GainHold CAM, 1MHz clocking. 0dBu input at 1KHz, Noise and distortion summed from 22Hz to 22KHz

Spurious Free Dynamic Range [8]	SFDR	-	100	-	dB	Unity-gain GainHold CAM and SnH output cell. 1MHz clocking. 0dBu input at 1KHz. See figure 7

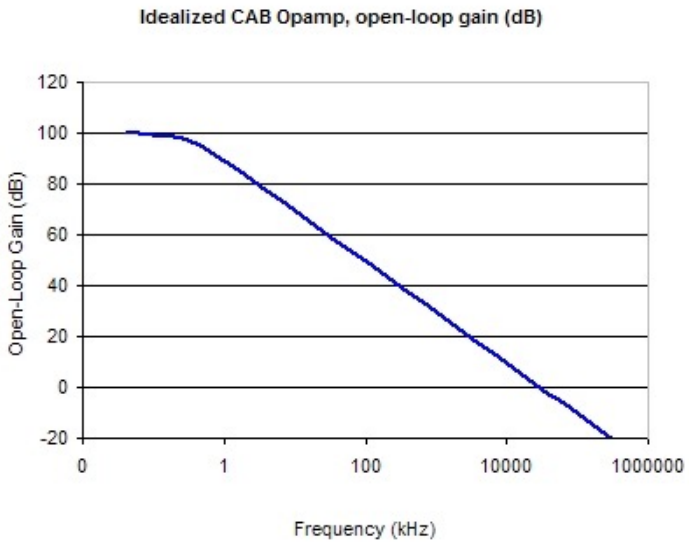


Figure 5: CAB Opamp Open Loop Gain Response

The idealized open loop gain plot is provided for information only. This information is associated with the dpASP in full power mode of operation. The dpASP operational amplifier open loop gain cannot be observed nor used when associated with external connections to the device. Internal reprogrammable routing impedances and switched capacitor circuit architectures using this operational amplifier limit the effective usable bandwidth.

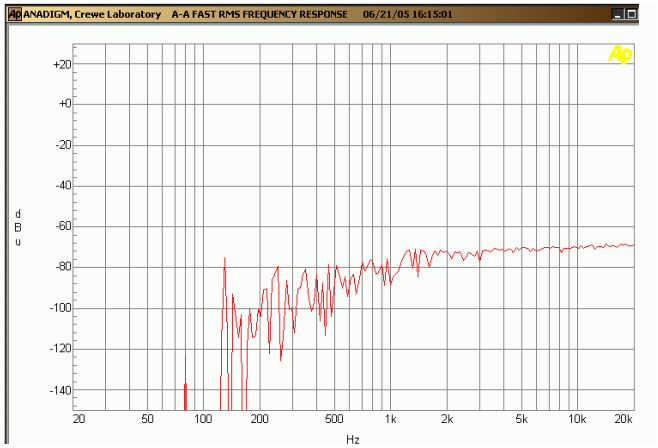


Figure 6: GainHold CMRR

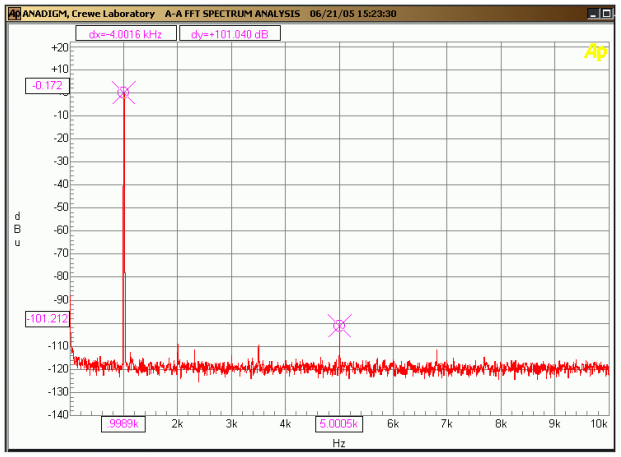


Figure 7:GainHold SFDR

CAB (Configurable Analog Block) Differential Comparator

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input Range, External or Internal	Vina	0.0	-	VDD	V	Will operate correctly.
Differential Input, Internal	Vdiffina	-	-	-	V	Set by internal signal clipping based on common mode voltage.
Differential Output **bypass** (bypass with core comparator is not a recommended operating mode)	VoutdiffL	0.163	-	3.138	V	3.3VDD. In digital output mode, 10KOhms connected between output pins. Varies with internal routing. Pad buffers are recommended in this mode.
	VoutdiffA	0.592		2.396		In analogue Vref level output mode. 10KOhms connected between output pins. Will vary with internal routing.
Input Voltage Offset	Voffcomp	-	0.78	1.22	mV	Zero hysteresis
Offset Voltage Temperature Coefficient	Voffsettc	-	1	-	µV/°C	from -40°C to 125°C, Zero hysteresis
Setup Time, Internal	Tsetint	-	-	125	nsec	
Setup Time, External	Tsetext	-	-	500	nsec	
Delay Time	Tdelay	½Td+25	-	1½Td+25	nsec	Td = 1/Fc Fc = master clock frequency
Output Load	Rload	10	-	-	Kohm	Applies if comparator drive off chip with output cell in bypass mode
Output Load	Cload	-	-	50	pF	Applies if comparator drive off chip with output cell in bypass mode
Differential Hysteresis	Hysta0	-	Voffcomp	-	mV	Hysteresis setting OFF
Differential Hysteresis	Hysta1	-	10	-	mV	Hysteresis setting ON
Hysteresis Temperature Coefficient	Hysttc1	-	10	-	µV/°C	Hysteresis setting = ON

ESD Characteristics

Pin Type	Human Body Model	Machine Model	Charged Device Model
Digital Inputs	4000V	250V	4kV
Digital Outputs	4000V	250V	4kV
Digital Bidirectional		4000V	250V	4kV
Digital Open Drain	4000V	250V	4kV
Analog Inputs	2000V	200V	4kV
Analog Outputs	1500V	100V	4kV
Reference Voltages		1500V	100V	4kV

The AN231E04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN231E04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Power Consumption – Various Modes

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Deep sleep mode [1a]	Idd	-	0.004	-	mA	VDD=3.3 volts, Tj=25°C
Stand Standyby mode [1b]	Idd	-	0.3	-	mA	VDD=3.3 volts, Tj=25°C
Small circuit mode [1c]	Idd	-	15	-	mA	VDD=3.3 volts, Tj=25°C
Nominal circuit mode[1d]	Idd	-	42	-	mA	VDD=3.3 volts, Tj=25°C
HighPower[1e]	Idd	-	61 67 73	- 75 -	mA	VDD=3.0 volts, Tj=85°C VDD=3.3 volts, Tj=25°C VDD=3.6 volts, Tj= -40°C
Temperature Coefficient for High power.	-	-	-2	-10	µA/°C	

1a. External clock stopped, all analog function disabled, memory active.
1b External clock at 16MHz on ACLK, all analog functions disabled, memory active.
1c. dpASP active elements – Gain hold CAM, One IO in SnH and both clocked at 1MHz, One IO bypass, all references on.
1d dpASP active elements - Four gain hold CAMs (4 CAB opamps), one CAB comparator, one CAB multiplier (1 CAB opamp, 1 CAB comparator, 1 CAB SAR ADC), Two IO in SnH, One IO in bypass, one simple IO in digital mode. 4 MHz clock for all, all references on.
1e dpASP active elements - Seven gain hold CAMs (seven CAB opamps), 1 arbitrary waveform generator (one CAB opamp, LUT, counter) 4 CAB comparators, 4 IO Sample and hold, references on, 4 MHz clock for all where possible, all references on.

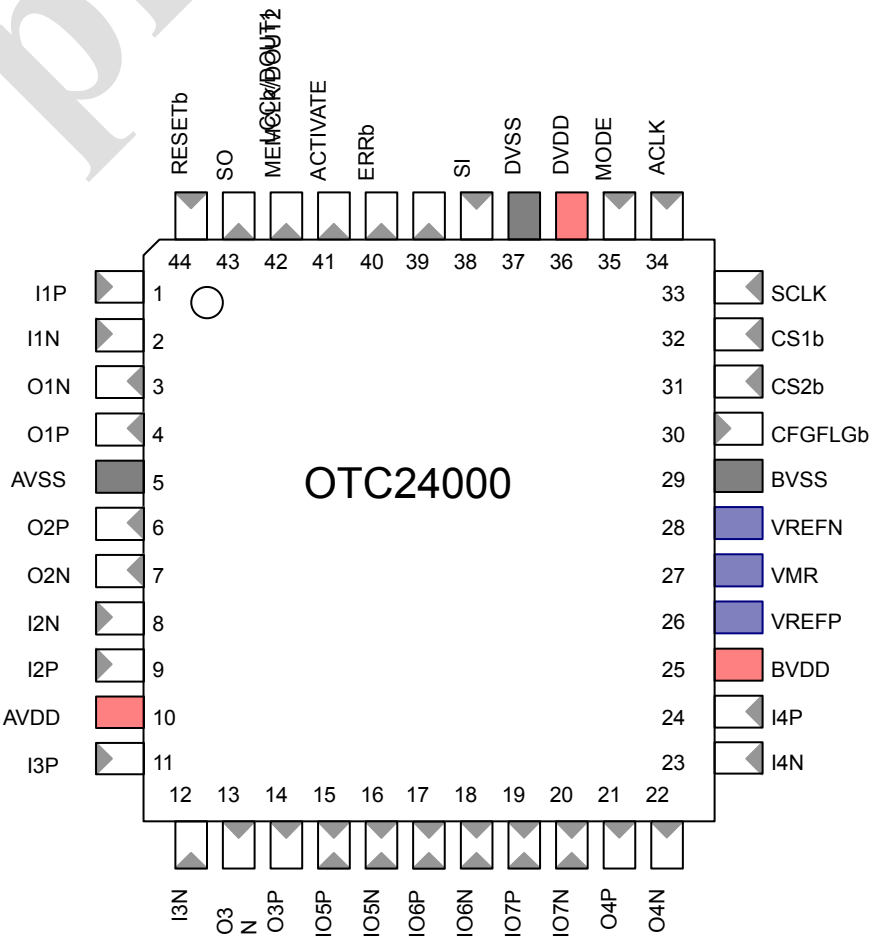
Pinout

Pin No.	Pin Name	Pin Type	Comments
1	I1P	+ve Input	Type1 Input/Output cell. (IO Cell 1) Analog or digital input and output pins
2	I1N	-ve Input	
3	O1N	-ve Output	
4	O1P	+ve Output	
5	AVSS	Ground Supply	Analog ground, 0 Volts
6	O2P	+ve Output	Type1 Input/Output cell. (IO cell 2) Analog or digital input and output pins
7	O2N	-ve Output	
8	I2N	-ve Input	
9	I2P	+ve Input	
10	AVDD	Positive Supply	Analog power 3.3 Volts
11	I3P	+ve Input	Type1a Input/Output cell. (IO cell 3) Analog or digital input and output pins
12	I3N	-ve Input	
13	O3N	-ve Output	
14	O3P	+ve Output	
15	IO5P	+ve Input/Output	Type 2 Input/Output cell. (IO cell 5)
16	IO5N	-ve Input/Output	
17	IO6P	+ve Input/Output	Type 2 Input/Output cell. (IO cell 6)
18	IO6N	-ve Input/Output	
19	IO7P	+ve Input/Output	Type 2a Input/Output cell. (IO cell 7)
20	IO7N	-ve Input/Output	
21	O4P	+ve Output	Type1a Input/Output cell. (IO cell 3) Analog or digital input and output pins
22	O4N	-ve Output	
23	I4N	-ve Input	
24	I4P	+ve Input	
25	BVDD	Positive Supply	Voltage reference power 3.3 Volts
26	VREFP	Reference load	Reference Voltage Noise suppression. Connected a 100nF capacitor from each pin to BVSS. The capacitive reservoir is used to sink and source peak current, thus reducing noise and maintaining stable reference voltages.
27	VMR	Reference load	
28	VREFN	Reference load	
29	BVSS	Ground Supply	Voltage reference ground 0 Volts
30	CFGFLGb	Digital Output	Config status pin. Open Drain Output with optional internal Pull-up resistor. The output voltage is also sensed by internal circuitry, See figure XX for schematic.
31	CS2b	Digital input	Chip select pin
32	CS1b	Digital input	Device select
33	SCLK	Digital input	CMOS, configuration logic strobe clock.
34	ACLK	Digital input	CMOS, Analog clock input
35	MODE	Digital input	Connect to VSS (ACLK and SCLK sourced externally). Connect to VDD (ACLK sourced externally, MEMCLK & SO generated internally).

36	DVDD	Positive Supply	Digital power 3.3 Volts
37	DVSS	Ground Supply	Digital ground 0.0 Volts
38	SI	Digital input	CMOS Serial data input.
39	LCCb/ DOUT1	Digital output	CMOS. Default function, Indicates Local Configuration Complete. Optional function (Single dpASP designs only), pin can be configured as user assignable signal path digital output under software control.
40	ERRb	Digital output	Error indication. Open Drain, External Pull-up resistor must be used (10KOhms) See fig XXa
41	ACTIVATE	Digital Output	Indicates Device activation. Open Drain Output with optional internal Pull-up resistor. The output voltage is also sensed by internal circuitry, See figure XX for schematic.
42	MEMCLK/ DOUT2	Digital Output	Outputs MEMCLK clock when MODE pin = VSS. Caution - Do not load this pin during reset (NOT to be pulled low externally)
43	SO	Digital Output	Serial Out, ONLY used as an output for SPI-PROM setup bytes during configuration.
44	RESETb	Digital Input	Connected to VSS to reset the dpASP. If held low the dpASP will remain in reset (2msec delay internal set-up time follows release of RESETb (when this pin is pulled high))

Mechanical and Handling

The OTC24000 comes in the industry standard 44 lead QFN package.
Dry pack handling is recommended. The package is qualified to MSL3 (JEDEC Standard, J-STD-020A, Level 3). Once the device is removed from dry pack, 30°C at 60% humidity for not longer than 168 hours is the maximum recommended exposure prior to solder reflow. If out of dry pack for longer than this recommended period of time, then the recommended bake out procedure prior to solder reflow is 24 hours at 125°C.
The package is compliant with RoHS and is Lead-free. Lead finish is Matt tin (Sn-Cu).



Symbol	Min	Nom	Max
A	0.90	0.9	1.00
A1	0.00	-	0.05
A2	-	0.2	-
D	6.925	7.00	7.075
D2	5.55	5.65	5.75
b	0.18	0.25	0.30
e	-	0.50	-
f	0.20	-	-
Note: Drawing and package conform to JEDEC			

QFN Package mechanical drawing.